THIN-FILM INTRACORTICAL RECORDING MICROELECTRODES

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Thin-Film Intracortical Recording Microelectrodes

Summary

The goal of this contract has been to develop a family of active recording probes suitable for fundamental studies in neurophysiology and for use in neural prostheses. The probes have 64 sites, of which eight can be selected for simultaneous use by the external world. On one of the probe designs (PIA-2B/3B), the neural signals are buffered and then passed directly off chip, whereas on the other (PIA-2/3) the signals are amplified, multiplexed, and then passed off chip to minimize external leads. Both two-dimensional (2D) and three-dimensional (3D) versions of these probes are being developed.

During the past term, we have continued the optimization of the probes for in-vivo use. Polypyrrole is being explored as one possible means for improving long-term site viability in-vivo. It can be applied by an electrochemical process similar to electroplating and so can be selectively deposited on desired sites. It may interact differently with the tissue than a metal site and the rather dome-shaped morphology of the site may also help in preventing tissue encapsulation. We have also constructed chronic probe assemblies compatible with use on guinea pigs that can provide continuous bias to chronically-implanted sites. During the coming term we hope to use this instrumentation to explore the effects of bias on tissue encapsulation of the sites. Polyimide secondary cables have also been developed for use with chronically-implanted probes in order to improve the robustness of these implants. These cables will be used in series with our normal silicon cables, which will provide greater flexibility over the final distance to the actual implant.

We are moving to demonstrate the ability to interface with these probes over a bidirectional telemetry link, eliminating all leads from the chronic assemblies. In this regard, we have completed a look at the use of subthreshold MOSFETs as shunt resistors at the amplifier inputs on the probes to prevent DC drift in the probe input voltage (and the associated problems this drift causes in data conversion and dynamic range in completely implanted systems). Such transistor clamps appear quite suitable for this application, attenuating the input DC drift from typical sites by a factor of almost 1000 while maintaining a flat frequency response from 100Hz to over 10kHz. The attenuation and frequency passband do not appear to be significantly affected by anticipated normal process variations, and so the technique appears viable for practical use. Telemetry circuits have been designed and simulated for use with the probes, including a voltage regulator, envelope detector, power-on-reset generator, and clock generator. The system will use a forward (input) frequency of 4MHz and a reverse (output) frequency of 25MHz with a range of operation of about 1cm. It will be implemented in a 1.2µm foundry CMOS process. Simulations suggest the above circuitry will dissipate about 8.3mW at 7.5V.

The first PIA-2B probes have also been completed. The probes are fully functional and are now being readied for in-vivo testing. Operated at 5V, they offer a per-channel output resistance of less than 10K ; use of a preamplifier based on a unity-gain opamp on the next iteration of this probe should drop the output resistance to less than 1K .

Thin-Film Intracortical Recording Microelectrodes

1. Introduction

The goal of this program is the realization of batch-fabricated recording electrode arrays capable of accurately sampling single-unit neural activity throughout of volume of cortical tissue on a chronic basis. Such arrays will constitute an important advance in instrumentation for the study of information processing in neural structures and should also be valuable for a number of next-generation closed-loop neural prostheses, where stimuli must be conditioned on the response of the physiological system.

The approach taken in this research involves the use of solid-state process technology to realize probes in which a precisely-etched silicon substrate supports an array of thin-film conductors insulated above and below by deposited dielectrics. Openings in the dielectrics, produced using photolithography, form recording sites which permit recording from single neurons on a highly-selective basis. The fabrication processes for both passive and active (containing signal processing circuitry) probe structures have been reported in the past along with scaling limits and the results of numerous acute experiments using passive probes in animals. In moving to chronic implant applications, the major problems are associated with the preserving the viability of the sites in-vivo (preventing tissue encapsulation of the sites) and with the probe output leads, both in terms of their number and their insulation. The probe must float in the tissue with minimal tethering forces, limiting the number of leads to a few at most. The encapsulation of these leads must offer adequate protection for the meg-ohm impedance levels of the sites while maintaining lead flexibility.

Our solution to the lead problem has involved two steps. The first has been to embed circuitry in the probe substrate to amplify and buffer the signals and to multiplex them onto a common output line. Using this approach, signal levels are increased by factors of over 100, impedance levels are reduced by four orders of magnitude, and the probe requires only three leads for operation, independent of the number of recording sites. A high-yield merged process permitting the integration of CMOS circuitry on the probe has been developed, and this circuitry has been designed and characterized. The second step has involved the development of silicon-based ribbon cables, realized using the same probe technology, to conduct the neural signals to the outside world. These cables have shown significant advantages over discrete leads, both in terms of the ease with which chronic implants can be assembled and in terms of the ability of the cables to survive long-term biased soaks in saline. The cables can be built directly into the probes so that they come off of the wafer as a single unit, requiring no joining or bonding operations between them. The cables are also significantly more flexible than previously-used discrete wire interconnects.

This contract calls for the development of active probes for neural recording. A 64-site 8-channel probe with site selection and signal buffering but no multiplexing is being developed (PIA-2B) along with a high-end multiplexed probe that includes gain (PIA-2). During the past quarter, we have done the following: 1) we have continued to fabricate passive probes for internal and external users; 2) we are exploring the use of polypyrrole as a way to improve long-term site viability; 3) we are developing secondary cables for use with shorter silicon cables in chronic implant situations and are preparing to test sites chronically under continuous bias; 4) we are continuing to develop circuitry for leadless probe operation; and 5) we have completed the first two- and three-dimensional active PIA-2B/3B recording probes. Work in these areas is discussed in the following sections.

2. Passive Probe Development

Long-Term Site Viability

During the past quarter, in a collaborative effort between the Center for Neural Communication Technology and Professor David Martin of the University of Michigan Material Science and Engineering Department, we have examined coating the iridium electrode sites with the conductive polymer polypyrrole. This is an electrochemical process and so it is selective to the probe sites in the same way metal electroplating would be. We have coated half the sites of a chronic electrode in this way. Figure 1 shows an example of a coated and an uncoated site on one probe. These probes will be implanted early in the next quarter, and we will follow their impedances and unit responses over time. This project is part of an effort to understand and control protein adsorption on the electrode surfaces. Polypyrrole gives many more options than a metal surface both chemically and morphologically (because of its rather domed, outward-projecting shape). Our hope is that the surface structure of the polypyrrole may provide better electrode integration with the neurons than iridium, due to its morphology, and that the unit responses and impedances will remain stable over a longer time frame.

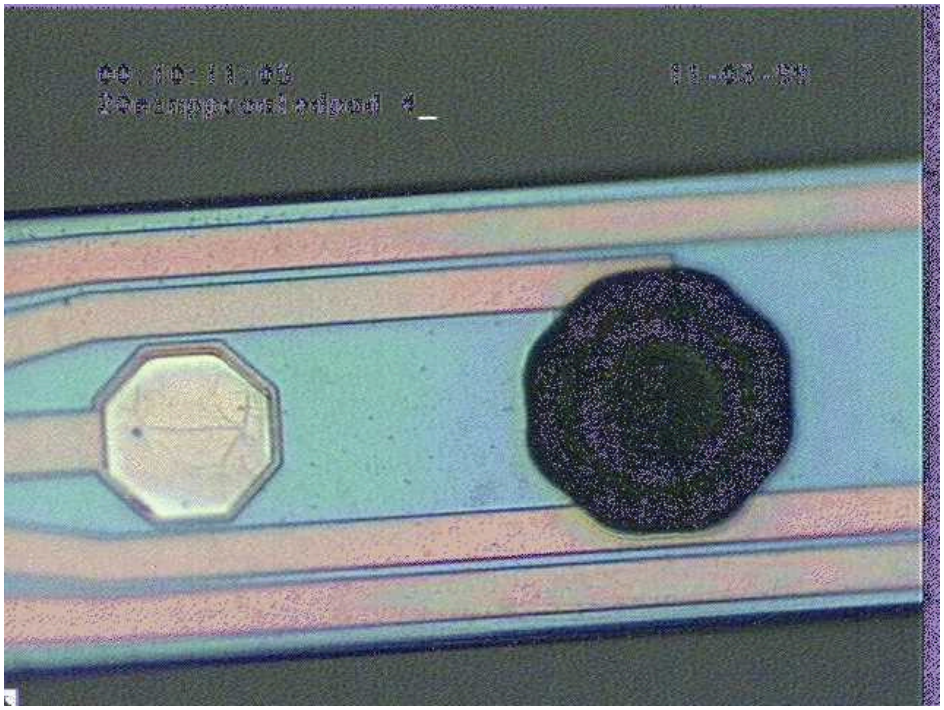

Fig. 1: Iridium oxide and polypyrrole sites on a passive probe. The polypyrrole is deposited by an electrolytic process so the deposit can be selective, depending on which site or sites receives current flow. Making electrodes for comparison experiments is therefore a simple post-processing step.

In another effort to maintain stable chronic recordings over a longer period of time, we are going to look at the effect of applying a continuous DC bias to an electrode site. A guinea pig will be implanted with a 3mm linear array electrode. The animal will then be fitted with a hat that will provide a constant +0.5V DC bias between one electrode site and a distant reference (Fig. 2). Another animal will be implanted as above, but will receive a -0.5V DC bias. The current delivered will be negligible in both cases. These animals will remain implanted for a period of three weeks, during which neural recordings and electrode impedance measurements will be routinely obtained. After this time, the animal will be sacrificed and examined histologically. It is known that electrical currents actively 'clean' the surface of

electrodes usually restoring the impedance characteristics. Often, but without great reliability, unit activity is restored. Thus far, experiments on this effect have been conducted by applying currents only for short intervals just before the electrode is to be used. This experiment is designed to determine if the continuous application of potential is fundamentally different than acute cleaning. The question is whether or not a fixed potential can be used to reduce (or enhance) site encapsulation. If the results here are positive, we will explore the parameter space (e.g., voltage range) more fully. The next step would be to perform the experiment with active recording probes (PIA-2B or STIM-2B) in which neural activity can be mimicked through stimulation. This will place an "artificial neuron" whose activity and position are known near the recording sites so that their ability to record over time can be assessed. We hope this will shed considerable light on the mechanisms for site failure in chronic situations.

Fig. 2: Representation of a chronically-implanted probe assembly that can be kept under bias on a guinea pig. The experiment is intended to allow the long-term behavior of recording sites to be studied in-vivo as a function of applied potential.

Packaging Developments

We have been investigating new connectors and cable technologies to increase the robustness and channel count in our chronic assemblies. As described in the last report, a hybrid cable technique is one option to gain increased strength and length from our interconnect. This technique uses a short length of silicon ribbon cable where maximum flexibility is critical (i.e., at the probe) and another cable where maximum mechanical strength and length are necessary (i.e., across the skull, under the skin, and up to the connector).

The North Carolina State University Biomedical Sensors Laboratory fabricated a prototype 16-channel polyimide cable for us during the last quarter. To form an assembly, the cable is attached to an 18-channel (extra two pins for ground connections) Omnetics Nano-pin connector with conductive epoxy. Exposed connections are coated with Epoxy Technologies 353ND-T. For the initial test structures, no probes were attached and the exposed bonding areas were coated with 353ND-T. The devices have been sent to Dr. David Edell for saline soak testing. After the first few weeks under soak, Dr. Edell reports that the cables are exhibiting low between-lead leakage currents although these currents are beginning to slowly increase. We hope to have more definitive results during the next quarter.

Another possible candidate for the secondary cable is a discrete-wire ribbon cable such as that manufactured by TempFlex, Inc. This particular product is an 8-lead flat cable made from copper wires (25µm diameter on a 100µm pitch) insulated with PFA. We currently have a sample of the ribbon and are investigating methods to cleanly strip the insulation to permit attachment of probes and connectors. Other wire materials, such as platinum, are an option as a custom order, and we will be investigating this further.

Until we have a hybrid cable technology that is proven, we will continue to use the silicon cable to study the chronic behavior of our electrodes. We have made a PC board to use with the Omnetics Nano pin connector and our new 16-channel chronic probe designs. A fully-assembled package is shown in Fig. 3. The package is assembled by first bonding the probe to the PC board and then insulating these connections with silastic. The connector is then soldered to the PC board, and a machined titanium percutaneous receptacle is epoxied around the connector. The entire device is finally coated with 353ND-T epoxy. A small piece of silastic tubing that has been cut in half longitudinally, placed around the cable, and then filled with silastic provides strain relief at the cable/PC board junction. The receptacle is threaded on the outside to accept a screw-on cap that will protect the small connector pins from the environment. Five devices have now been completed and will be implanted in the coming weeks.

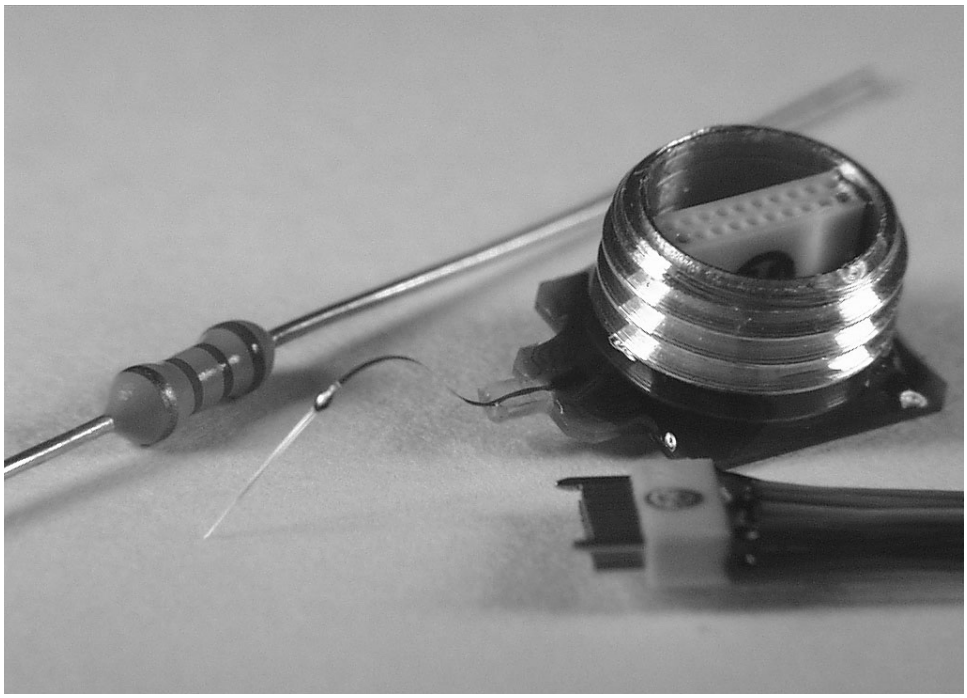

Fig. 3: A new 16-channel chronic assembly. The titanium receptacle is threaded to accept a screw-on cap. The outer diameter of the receptacle is ~1cm. The connector mate has two guide pins to simplify plug-in.

The probe in Fig. 3 is from the new STANDARDS mask set outlined in the last report. This mask includes 11 different chronic designs, which vary in shank length, site spacing, and number of shanks. This particular design, the 5mm100_chron, has 16 sites spaced at 100µm intervals on a 5mm shank. A photograph of the tip is shown in Figure 4.

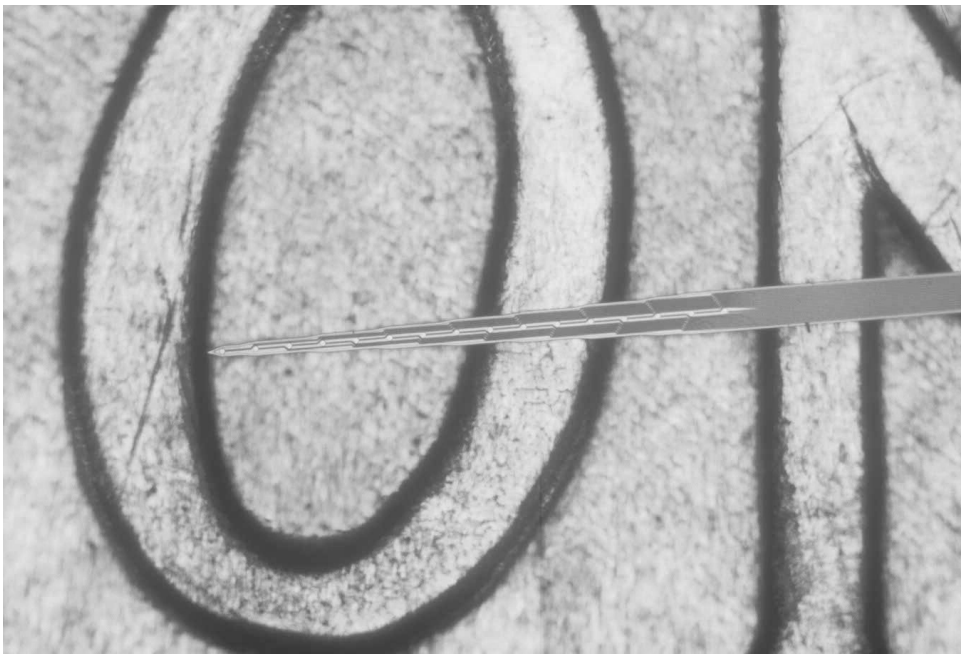

Fig. 4: Tip of the probe used in the chronic implant shown in Fig. 3. This design is one of 11 new chronic probe designs included on the mask set, STANDARDS. The probe is laying on the backside of a penny over the word "ONE". The sites are spaced at 100µm intervals.

3. Development of Circuitry for Leadless Probe Operation

This project seeks to develop probe readout circuitry and a telemetry interface that will allow one or more probes to be operated leadless, with a two-way telemetry link between the intracranial platform and the outside world. During the last quarter, work has been carried out on the following tasks:

1. Completion of the final tests on the input DC stabilization circuitry; and
2. Design and simulation of the circuit blocks of a telemetry system for multichannel neural recording applications.

3.1 Testing of the New DC Stabilization System:

Figure 5 shows a schematic representation of the new DC stabilization system that was recently fabricated through the MOSIS service. The operation of the circuit, simulation results, and a die photograph, were presented in previous reports.

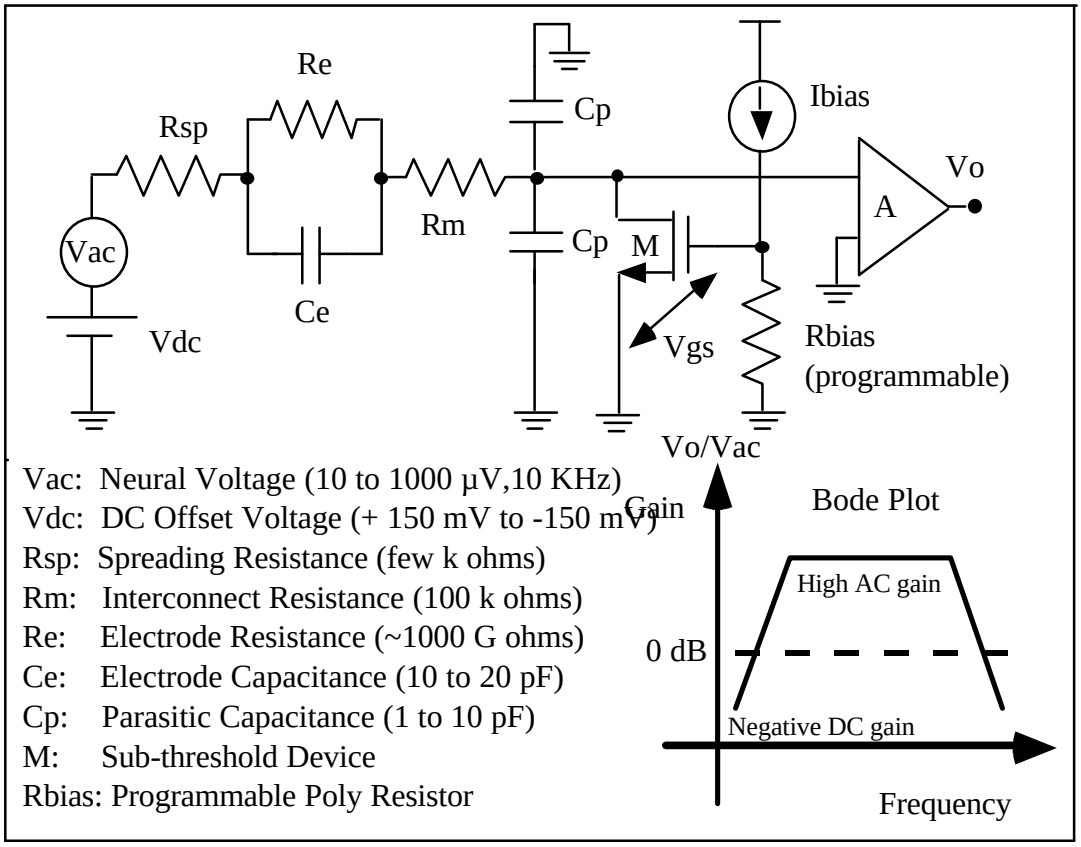

Fig. 5: Schematic of the electrode-electrolyte interface and the DC stabilization system.

As shown in Fig. 5, the DC stabilization system consists of two parts: a front-end sub-threshold biased NMOS transistor (M), and a 3-stage DC feedback amplifier (A). The NMOS transistor essentially acts as a voltage-variable resistor (with drain-source resistance Rds) that attenuates the DC offset (Vdc) in the recorded signal (Vac), by resistive division. At the same time, it keeps the cut-off frequency of the high-pass filter formed by Ce-Rds below 100 Hz. Ideally, the system should offer at least 40 to 50 dB of DC attenuation in the stop band (DC to 100Hz) and high AC gain in the pass band (100Hz to 20kHz). The expected frequency response of the system is also shown in Fig. 5, illustrating the expected AC response of the system.

AC and DC Test Results of the System

In order to characterize this new system, a simple test setup has been used. The circuits are connected to passive probes (either gold or iridium recording sites) and the probe is then inserted into a saline solution. The solution is driven using a large platinum electrode (which functions as a working electrode) using a DC supply voltage and an AC source, which are connected in series. Note that in such a setup one can change both the DC and the AC voltages to mimic actual changes that may be encountered in biological applications. Figure 6 shows the measured DC response of the stabilization-amplifier system interfaced with iridium recording probes in saline (with linear fits to the measured results).

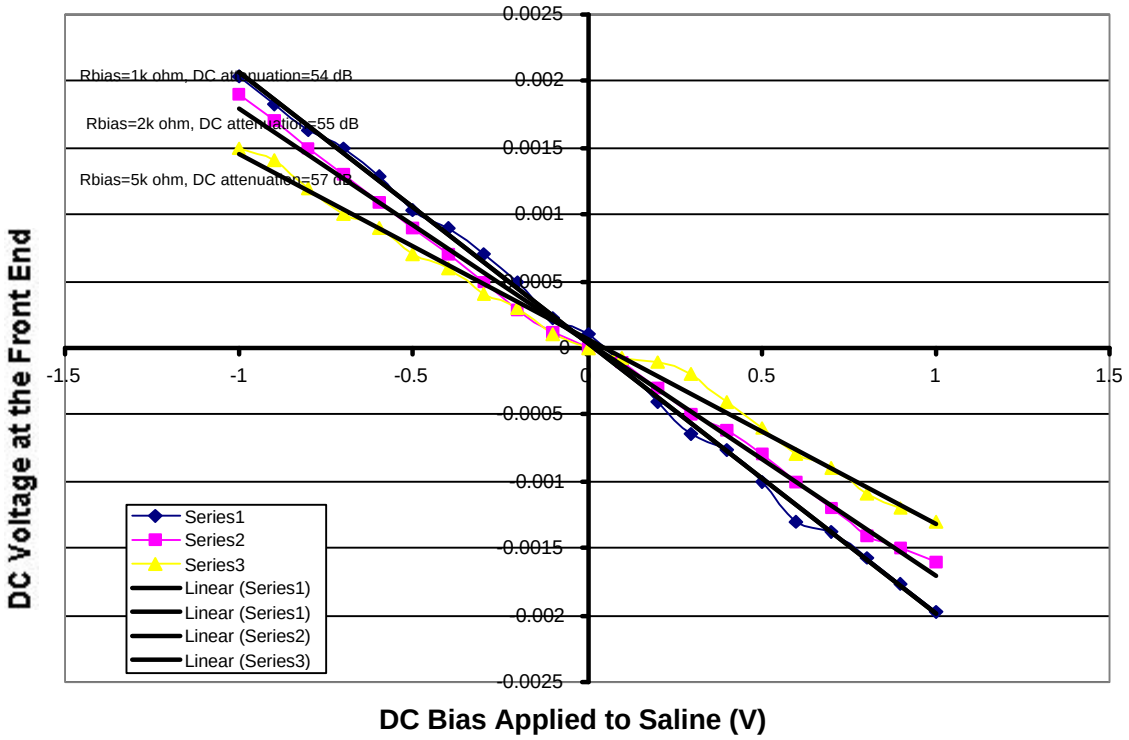

Fig. 6: DC response of the front-end stage, showing the effect of variable bias set by trimmable resistor Rbias (equal to 1, 2, and 5k).

Note that the voltage at the front end of the circuitry can be controlled by changing the DC voltage in the DC supply that is connected to the saline solution through the large working electrode. As can be seen, the response of the sub-threshold device (and hence of the entire system) is dependent on the biasing resistance Rbias. In order to be able to change the bias voltage, especially for test purposes, Rbias has been made trimmable. As Rbias is increased, Vgs increases, the drain-source resistance of M (Rds) decreases and this increases the DC attenuation of the system. The variation in DC attenuation in response to changing Rbias can be seen in Fig. 2. As the value of Rbias increases from 1k to 5k , the DC attenuation (slope of the transfer curve) increases from 54dB to 57dB, as shown. Note that in the final system one will not need to adjust this slope. The attenuation noted here is nearly 1000x, which means that a 0.25V offset at the input would be attenuated to about 250V, which is well within the normal dynamic range of a probe amplifier. Thus, this technique appears capable of resolving the front-end bias instabilities that are sometimes seen. Further, the attenuation is not so sensitive to the precise values of Rbias that control in processing would appear to be a problem.

Fig. 7 shows the measured frequency response of the fabricated test system. The frequency of the input AC signal was swept from 10Hz to 20kHz and the output of the amplifier was measured on an HP4194A Gain-Phase Analyzer. The plot shows that the DC attenuation at 59Hz is about 16dB, with the AC gain rising to about 35dB in the pass band (100Hz to 15kHz). This clearly indicates that the AC cutoff of the system is below 100Hz, which, as mentioned earlier, is an important requirement of the system. The AC gain as shown in the Bode plot is in close agreement with measurements made an oscilloscope, which are seen in Fig. 8 below. Here, the saline solution was driven by a sinusoidal signal (associated with a variable DC offset) and the amplified output was noted. The DC offset was then varied from 0V to 1V, and the change in the DC voltage at the output was measured.

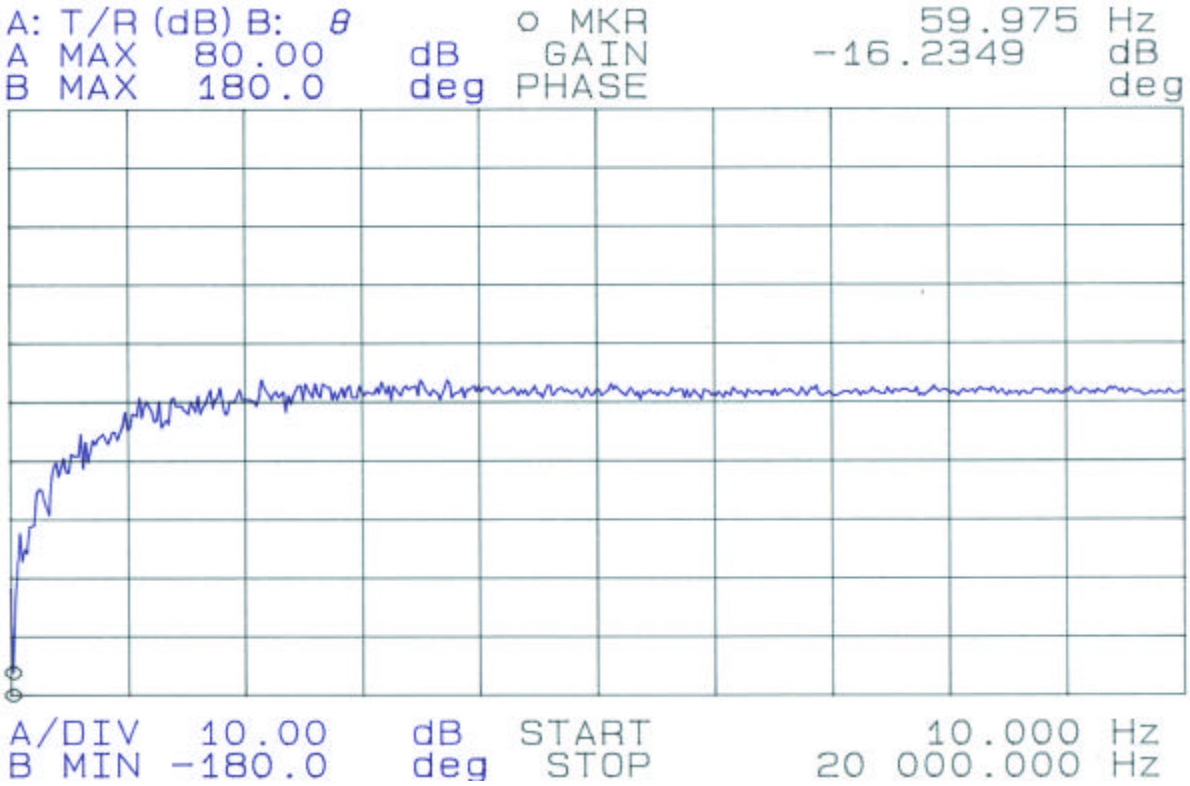

Fig. 7: Bode Plot showing the frequency response of the DC stabilization system.

Figure 8 shows that the AC gain of the system is about 38dB. However, this value is less than the AC gain obtained through simulations (about 55dB). This is believed to be due to the rather large deviation in the actual value of the threshold voltage on the NMOS transistors from those assumed in the simulations. This threshold voltage was significantly different than what the provider of this process had indicated. MOSIS has not indicated to us why such a large shift in the threshold was obtained in this run. In their normal specifications the shift in process parameters is relatively small and the circuitry was designed to withstand the expected variations in process parameters.

Based on these results, we feel that the new DC stabilization circuitry performs quite well and can be used in future designs of the recording probes. A modified and final design of this circuitry will be used in the layout of the circuitry that is being designed for the telemetry circuitry.

3.2 Design of a Telemetry Platform For Recording Probes

As mentioned in previous quarterly report, work has continued on the design of a two-channel "Telemetry IC". It is anticipated that such an IC would later serve as a platform that can be interfaced with an active recording probe. Note that the main objective of this current design is to build all of the necessary circuit blocks for such a telemetry chip in CMOS using standard foundry processes. Similar telemetry circuitry has been designed by our group in a BiCMOS process that we run here at Michigan, but this process is not easily scalable to feature sizes below 3µm. The current telemetry circuitry is being designed for interfacing with a passive recording probe. It is believed that such a scheme will enable a

better understanding of some of the vital issues and trade-offs associated with the design and provide valuable inputs for future designs.

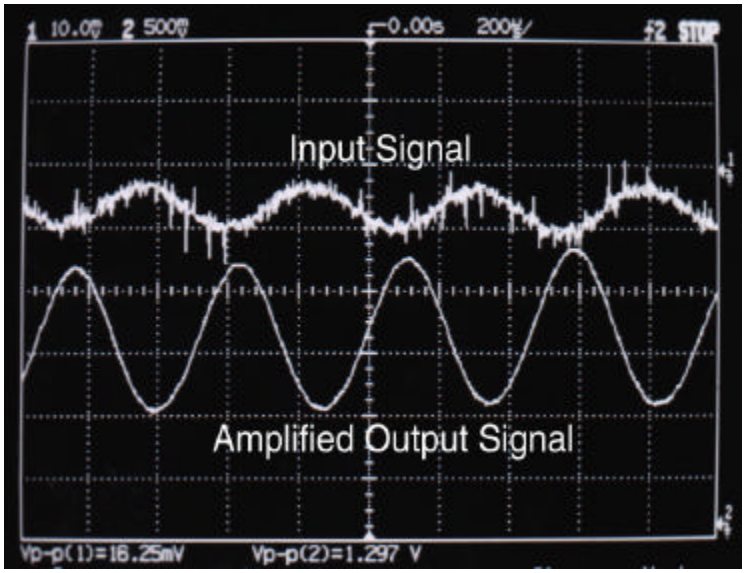

Fig. 8: AC performance of the system showing amplification of an input signal.

Figure 9 shows the main circuit blocks of the system. It is desired to operate the circuit from an external interface that consists of a Class E amplifier which supplies RF power and data to the system. The RF signal is captured, rectified and demodulated to obtain the necessary power and control for the system. The recorded, stabilized and amplified signal is multiplexed and digitized before being transmitted out to the external interface. Table 1 shows some of the important circuit specifications.

Table 1: Important Design Specifications of the Telemetry System

SPECIFICATION	***VALUE***
FREQUENCY (FORWARD)	4 MHz
FREQUENCY (REVERSE)	> 25 MHz
TYPE OF PROBE	32 SITE (PASSIVE), 2 CHANNELS SELECTED
RANGE OF OPERATION	~1 cm
TECHNOLOGY TO BE USED	1.2 µm Foundry CMOS

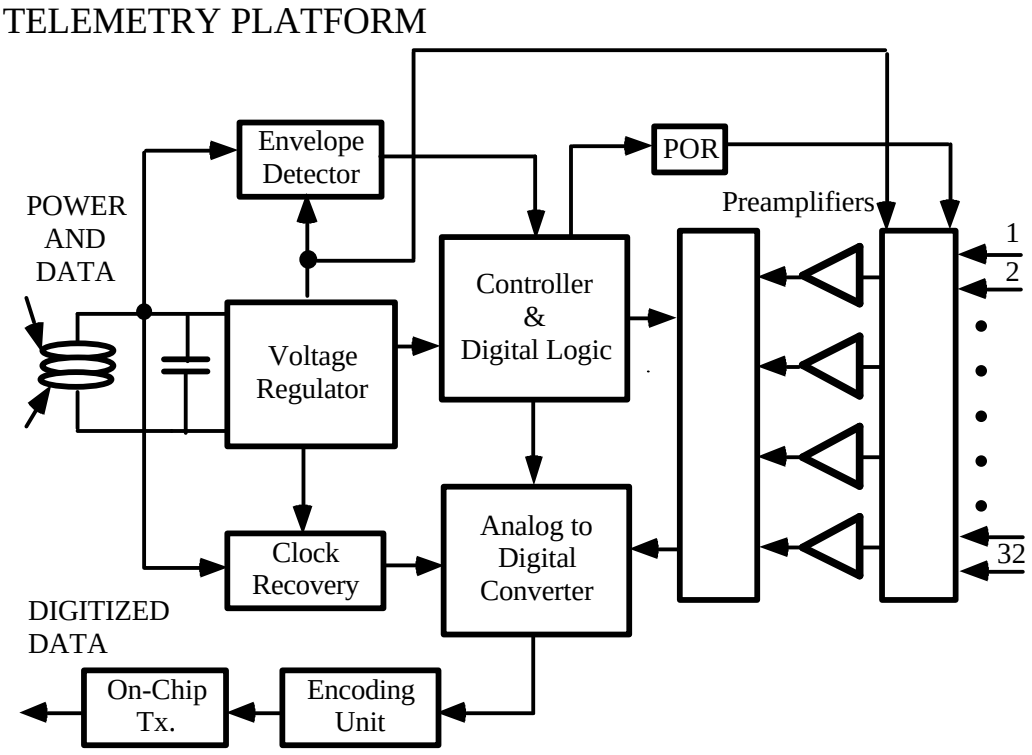

Fig. 9: Schematic of the proposed telemetry chip.

The design and simulation of the various blocks of this circuitry is underway. Thus far, the following circuit blocks have been successfully designed and simulated: the voltage regulator, envelope detector, power-on-reset generator, and the clock generator. These circuit blocks comprise the analog front-end of the IC and have to be carefully designed since they will be subjected to high RF voltages and are the most power-hungry section of the overall system.

Design and Simulation of a 5V CMOS Voltage Regulator

Figure 10 shows the circuit schematic of the proposed voltage regulator, which is implemented as a 2-stage circuit. The input RF signal drives a supply-independent current source (shown in Fig. 10). The current flowing in the current source is determined by the ratio of the differences in the base emitter voltages of the substrate pnp transistors and the resistance R_{bias}. Thus:

$$I_{bias}=I_{diode}=\Delta V_{be}/R_{bias}$$

To first order, the current in the diode string, I_{diode} is independent of supply variations and can be used to generate a voltage reference Vref. Vref is then supplied to the 2nd stage, which is a non-inverting circuit consisting of the opamp and the resistors R1 and R2. Thus the output voltage now only depends on V_{ref}, R1 and R2 all of which are constant. Thus, V_0 is given by

$$V_0=V_{ref}(1+R1/R2)$$

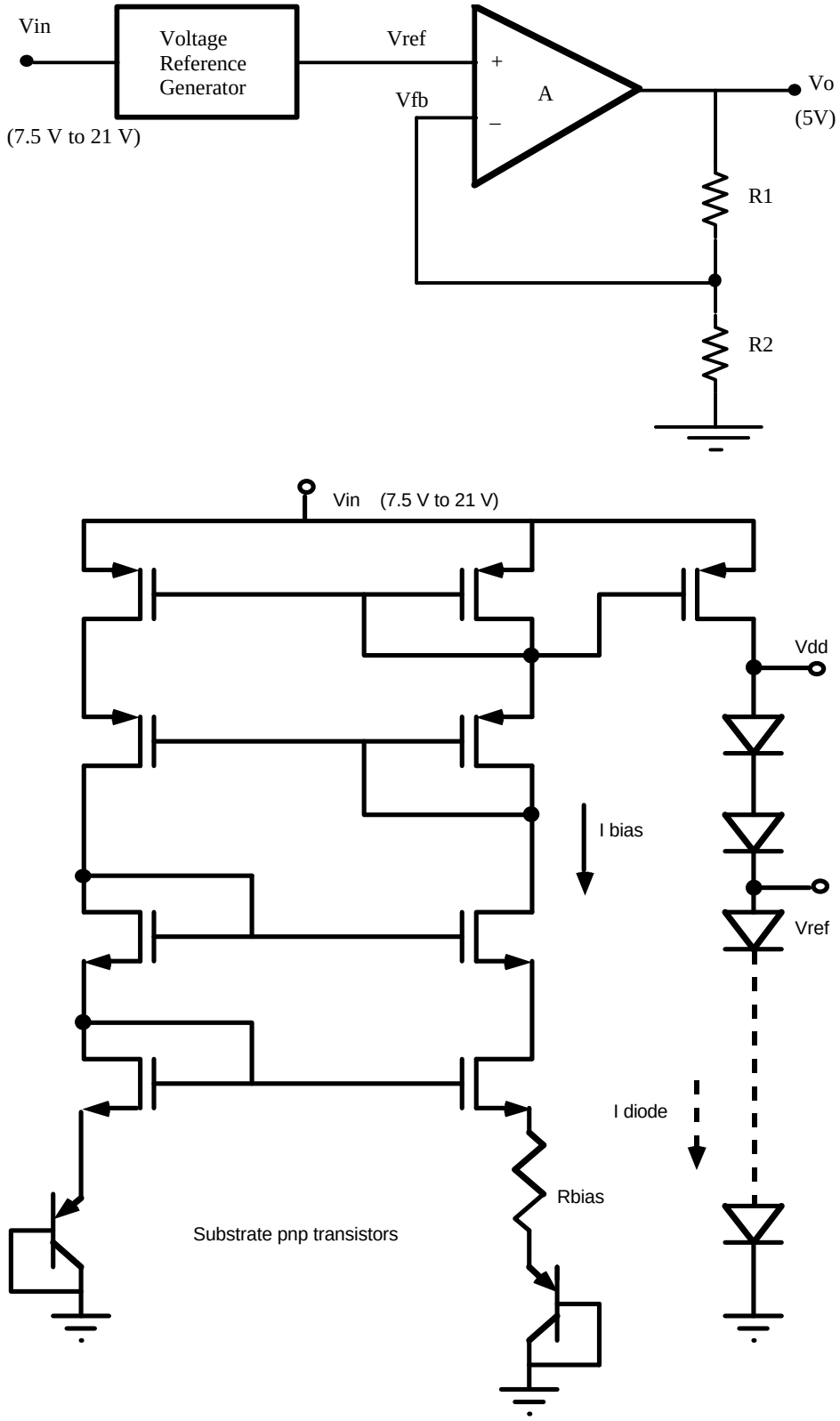

Fig. 10: Schematic of the voltage regulator and the reference voltage generator.

Fig. 11 shows the simulation results of the voltage regulator circuit (all simulations were performed in HSPICE level 3, using model files provided by MOSIS). The top panel shows the input Amplitude Modulated (AM) signal that is received by the circuit. The AM signal has a peak amplitude of

10V. The bottom panel shows the 5V output of the regulator. It should be noted that the input signal may range anywhere between 8V and 20V. The voltage regulator requires at least a 7.5V input in order to generate a 5V output. The reason for this is that the rectifier uses a pair of diodes which take up 1.4V of the received signal. The circuit is designed in n-well CMOS and dissipates approximately 5mW of power at 7.5V.

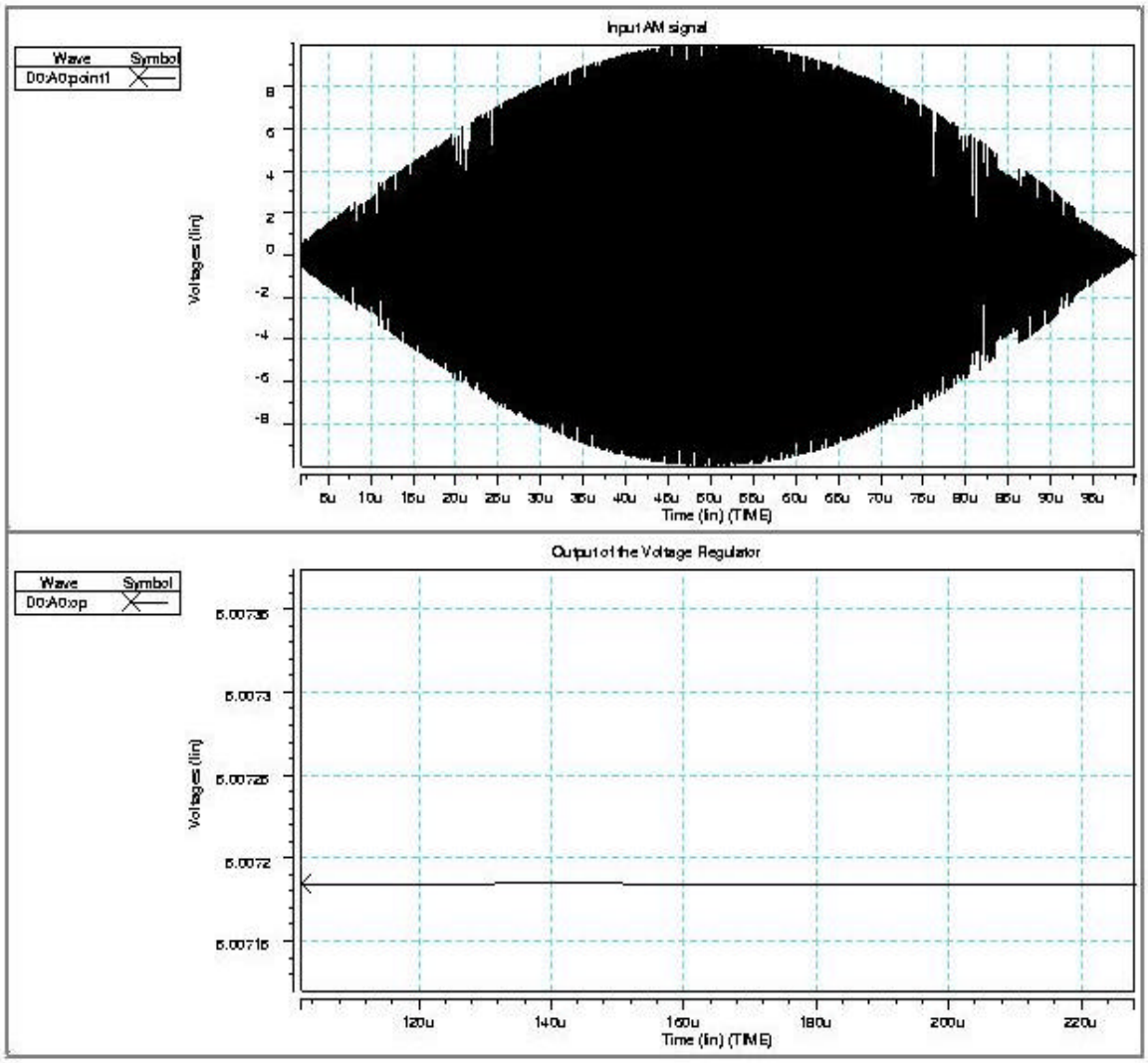

Fig. 11: HSPICE simulation of the voltage regulator.

Design and Simulation of Envelope Detector

Figure 12 shows the schematic of the envelope detector. The circuit consists of an arrangement of current mirrors. In the steady state, the currents flowing in the branches of the current mirror are perfectly balanced. However, when the rectified signal is applied, the currents flowing in opposite arms of the current mirror are perturbed from their quiescent values due to the fact that capacitors C1 and C2 have different values.

The RC time constant of the circuit must be comparable to the time-period of the RF carrier wave in order to ensure that the envelope is recovered. This change in current is sensed and is used to generate

0-to-1 and 1-to-0 transitions like a comparator. The output is then buffered using a series of inverters to generate a clean square wave with a 50 % duty cycle.

The simulation results for the envelope detector are shown in Fig. 13. The top panel shows the full wave rectified signal that is offset from ground by two diode drops. The bottom panel shows the square wave output of the envelope detector. The circuit can be designed to include additional inverters in the chain in order to generate a clean square wave with a 50% duty cycle. The circuit consumes 2.79mW of power at a supply voltage of 5V.

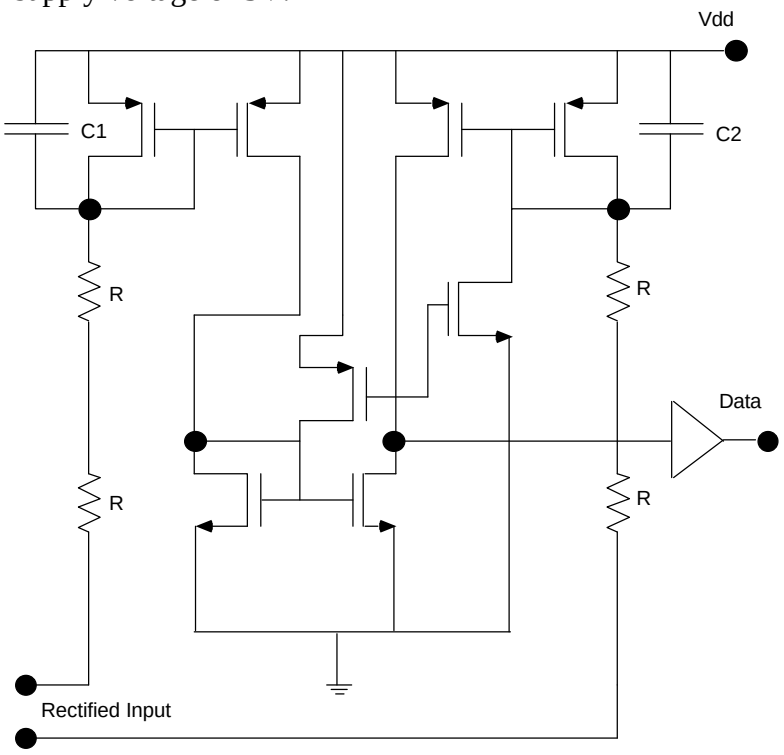

Fig. 12: Circuit schematic of the envelope detector.

Clock Generator

The circuit schematic of the clock generator is shown in Fig. 14. The clock generator is a simple circuit that is designed to generate a square wave from the received RF signal. Initially, the frequency of the clock signal is equal to the frequency of the full wave rectified signal (which in turn is twice the frequency of the RF carrier signal). However, this need not be at the desired frequency. Thus, a "divide by n" counter may be employed to divide down the frequency to the desired value at which the clock signal is to be generated. In the current simulations, the counter has not been included. It will be incorporated in the design at a later stage.

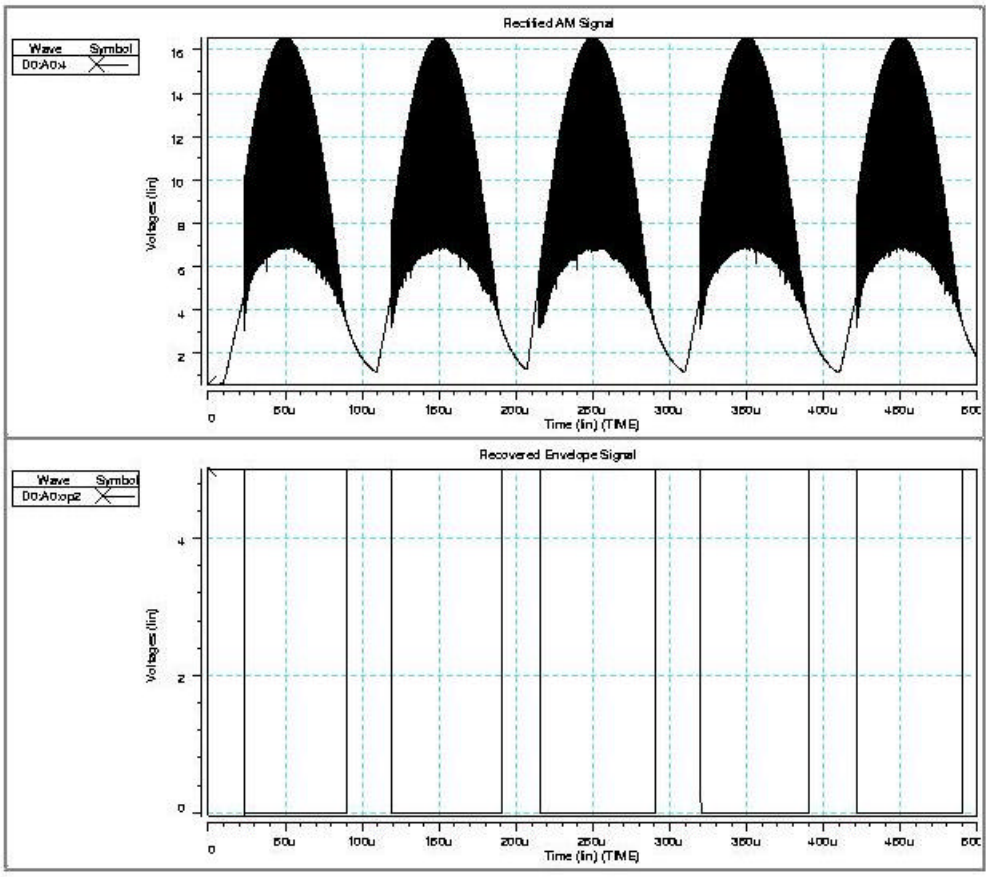

Fig. 13: HSPICE simulation of the envelope detector.

The input AM signal is rectified using a diode bridge circuit. Since the received signal may have a high peak voltage (which could damage the MOS transistors) it is necessary to divide the voltage down, using a pair of capacitors, C1 and C2. The received signal is then sent through a chain of inverter buffers. The inverters are biased near their trip point, which is in the region of 2.5V. Thus any rectified signal will trigger the inverters, resulting in a square wave. The signal passes through a chain of inverters which produces a clean square wave with a 50% duty cycle. As mentioned before, a counter can be connected to the output of the clock generator in order to modify the frequency of the clock signal.

Fig. 15 shows the results of the simulated clock generator circuit. The top panel shows the full-wave rectified signal, while the bottom panel shows the generated clock signal. Since the input RF signal is at a frequency of 4MHz, the clock signal has a frequency of 8MHz. The circuit consumes 0.4μW of power at a 5V supply.

Power-On-Reset (POR)

The Power-On-Reset circuit is used with the envelope detector mentioned earlier. This is shown in Fig. 16 and consists of three parts: an input inverter, a static RS flip flop consisting of two cross coupled NMOS devices and an output inverter. At power-up POR output is set to a high voltage due to the size difference in transistors in the RS flip flop. When the first low signal is received at the "DATA" input, the output of the POR goes low and stays there for the rest of the operation of the system. The Power On Reset is needed to reset the logic circuitry of the system during power up. If this is not done,

some spurious value may be contained in the digital logic system and this may cause the system to malfunction. The POR circuit resets the system and prevents this from happening. The POR circuit consumes 0.48mW of power at a supply voltage of 5V.

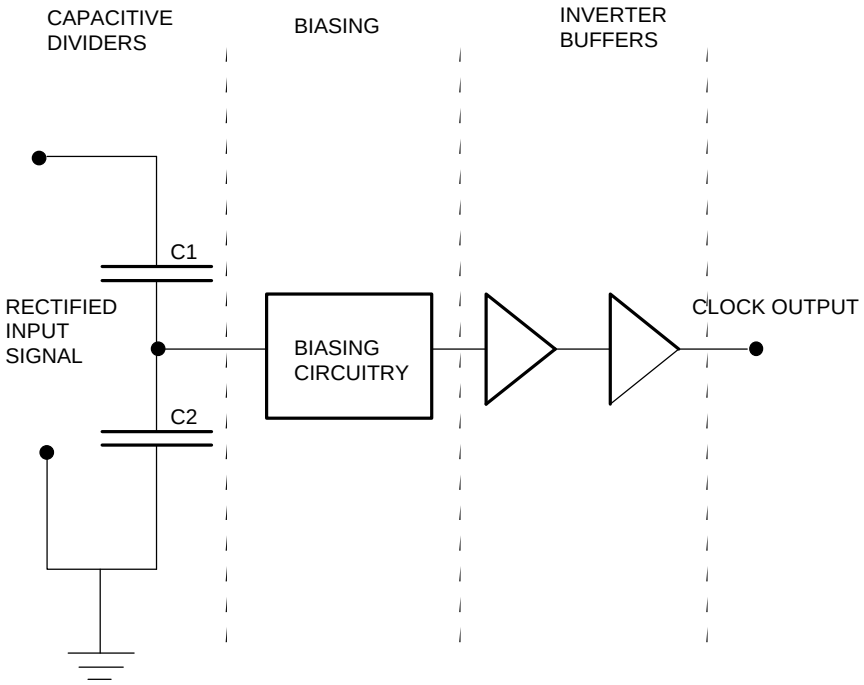

Fig. 14: Schematic of the clock generator.

In the coming quarter, we will continue to design and simulate the rest of the circuit blocks of the telemetry unit and finish the layout for this circuitry. If the layout is completed, it will be sent out to MOSIS for fabrication.

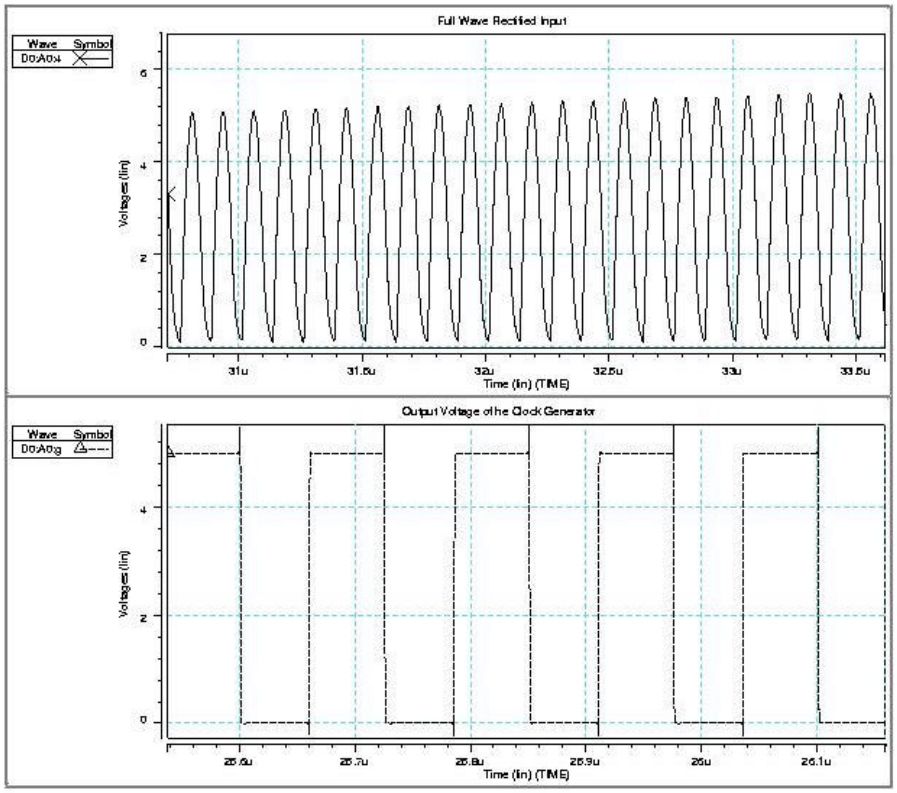

Fig. 15: HSPICE simulation of the clock generator.

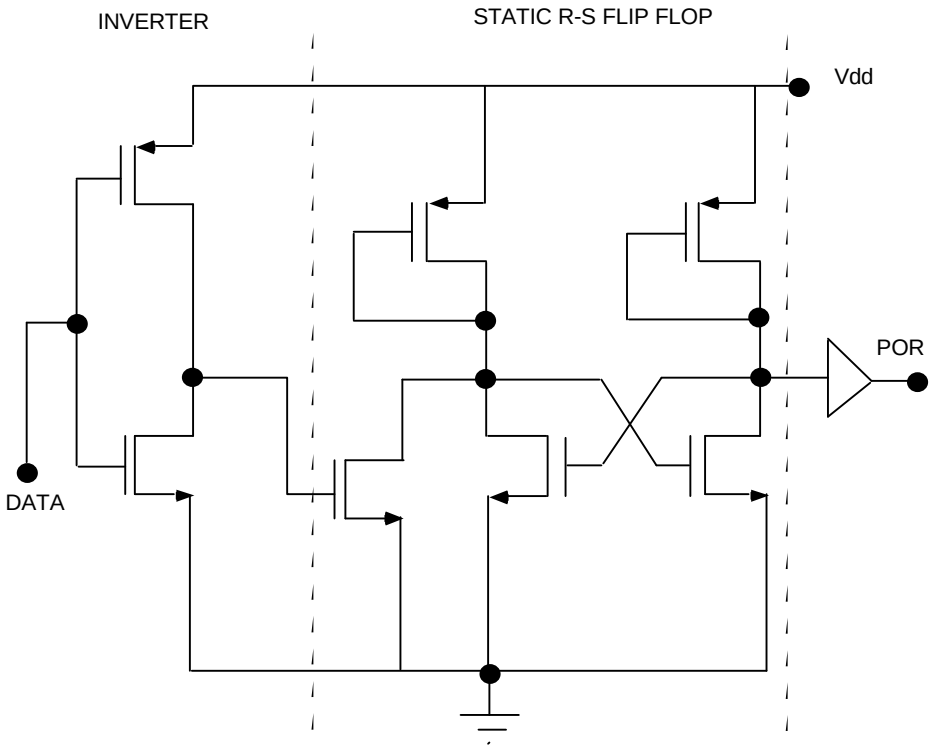

Fig. 16: Schematic of the power on reset circuit.

4. Development of a 64-Site Eight-Channel Non-Multiplexed Recording Probe (PIA-2B)

The architecture and design of a 64-site front-end-selected and buffered probe have been discussed in previous quarterly reports. During the past quarter, work has progressed on the final preparation of the probes for implantation and in-vivo testing. The probes were etched out and bonded, and in-vitro testing was begun. The correct functioning of the active circuitry was confirmed after etching and bonding, and the performance of the buffers has been tested.

The circuit areas were protected during the EDP release with a front-side dielectric mask, which included corner compensation and dielectric bridges. The yield loss during etching was minimal, although some attack of the probe corners was noted. Causes of this attack will be explored, although in most cases the etch did not proceed far enough to damage the circuit areas. Inspection under a light microscope shows that the probe shanks are etched all the way to the etch stop and are suitable for insertion into tissue. A dish of etched probes is shown in Fig. 17 below.

Fig. 17: A dish of probes etched from the wafer ALB5.

PIA-2B has a total of twelve input and output pads, including the eight recording channels, the serial-data-in channel, the off-chip clock input, and the power rails. The probes were bonded to a twelve-pin PC board connector of the type used regularly for passive probes. This package will allow for testing of the probe using the same head-stage amplifier and preamplifier which is already used for implantation and recording from passive probes and will thus allow for direct comparison of buffered and unbuffered recordings. Testing of the on-chip digital circuitry was carried out on the completed packages, and correct functionality of the circuitry was verified with receipt of the "I'm Okay" signal from the probe (see Fig. 18.)

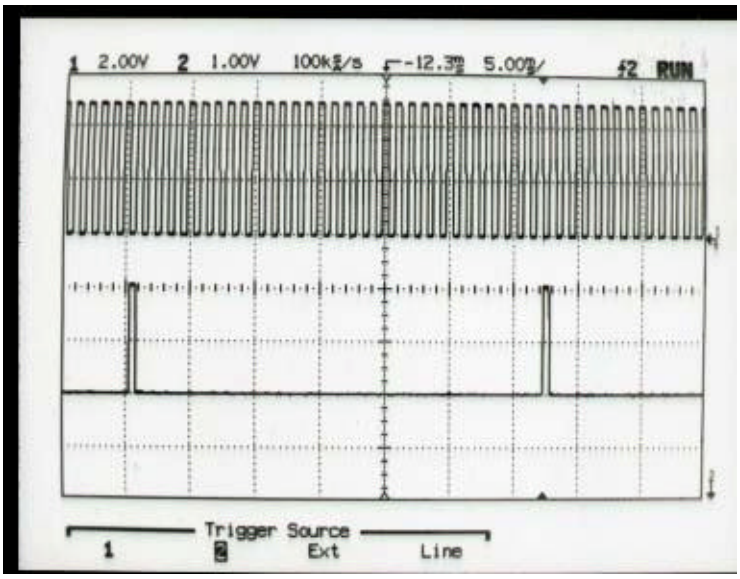

Fig. 18: The "I'm Okay" signal from a completed PIA-2B probe.

Testing of the buffer performance was carried out both in a benchtop set-up and in a saline environment. First, direct electrical connections were made to the source-follower buffers, and the output impedance was measured as a function of supply voltage. Figure 19 gives the buffer output impedance as a function of supply voltage, which can be compared to the curve from simulations which was given in a previous quarterly report and is given again here on the same axes. We can see that at a supply voltage in the range 3.5-5V, we achieve a decrease in output impedance of nearly two orders of magnitude when compared to the typical 1MΩ impedance of a 100μm^2 (unactivated) irridium site. The buffers were also tested in a saline environment; a 100mV signal injected into the saline is shown in Fig. 20 below. The gain is found to be approximately 0.88, with an upper corner frequency (at Vdd= 5 volts) of 400kHz.

A degradation of probe performance was noted with repeated exposure to saline; it is possible that the circuits were affected by the exposure to sodium and/or potassium after immersion. The pad areas were protected with EPO-TEK type 302 epoxy, but the circuit areas themselves were covered only with the LTO deposited on top of the final circuit interconnect layer. This problem will be addressed by covering the circuit area with epoxy, and by exploring different types of bonding epoxy if necessary. In addition, more care will be taken in the rinsing of the probes after use. It is important to note that the probes so far under test are intended for use in acute assemblies and therefore no special measures such as metal shielding have been used to support chronic immersion in saline.

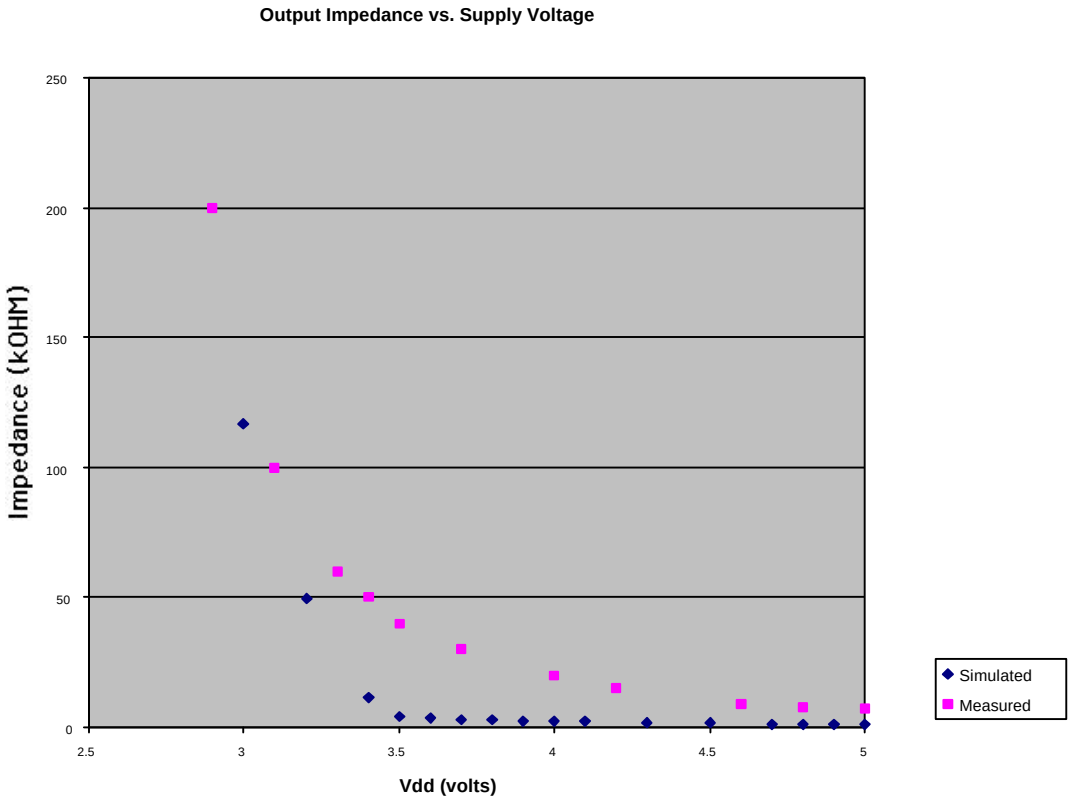

Fig. 19: Buffer output impedance according to simulation, and as measured on the fabricated probes.

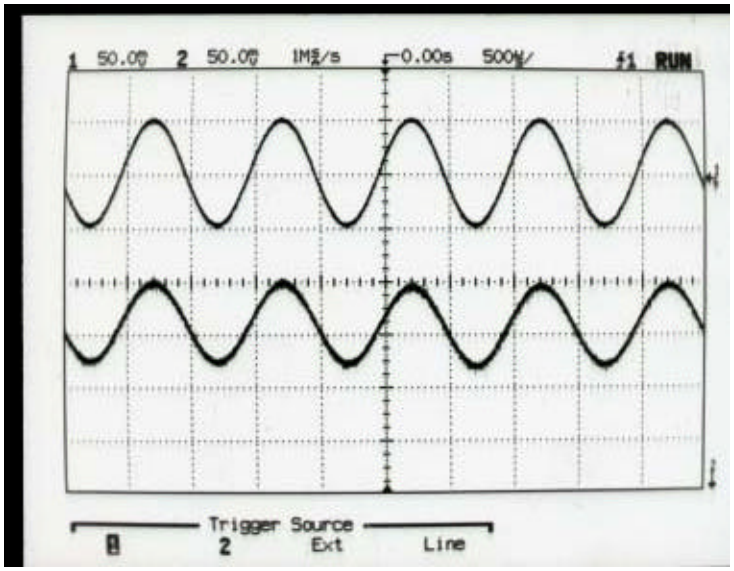

Fig. 20: A 1kHz test signal applied to saline (top) and recorded on a buffered probe channel (bottom.)

A completed sixteen-shank PIA-2B probe after etching, resting on a penny for size reference, is shown below in Fig. 21. During the coming quarter, the performance of the buffered recording channels in-vivo will be explored by implantation in guinea pigs. A comparison of buffered and unbuffered channels will be made both by switching the buffers in and out, and by comparing the buffered probes

with the performance of passive probes in the same preparation. An interface unit will be designed to load the probes with site configurations and allow recording from all available sites. It should also be noted that the 96-site buffered active probe fabricated for Dr. Gyorgy Buzsaki was also successfully completed on this mask set. We are preparing to test these probes in an acute preparation and will then send the probes to him for use in-vivo.

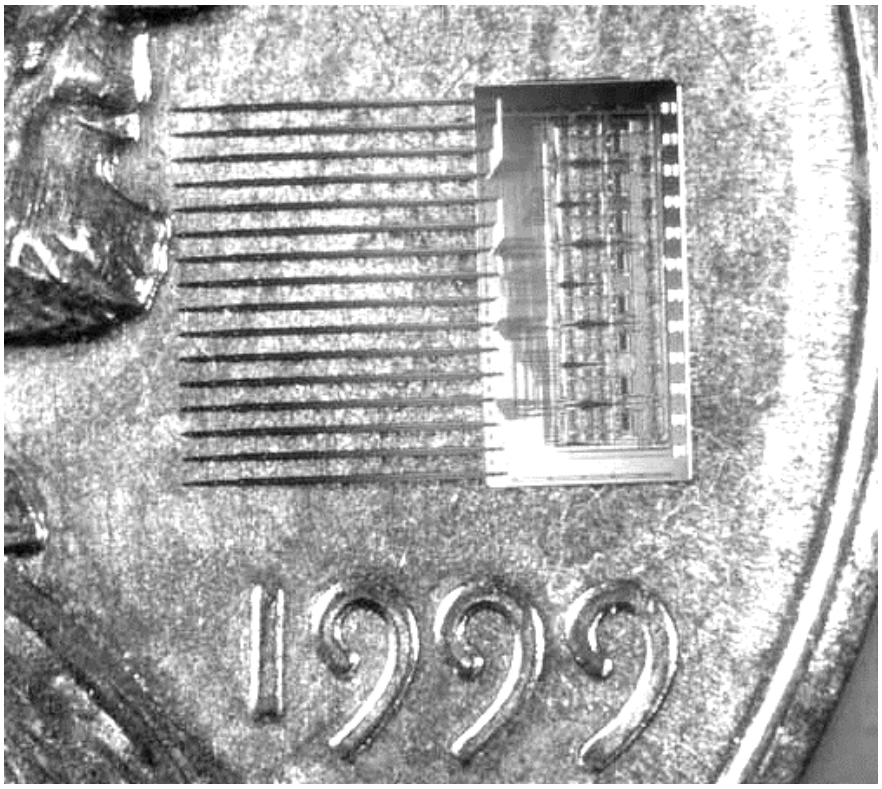

Fig. 21: PIA-2B after fabrication and final etching.

5. Conclusions

During the past term, we have continued the optimization of the probes for in-vivo use. Polypyrrole is being explored as one possible means for improving long-term site viability in-vivo. It can be applied by an electrochemical process similar to electroplating and so can be selectively deposited on desired sites. It may interact differently with the tissue than a metal site and the rather dome-shaped morphology of the site may also help in preventing tissue encapsulation. We have also constructed chronic probe assemblies compatible with use on guinea pigs that can provide continuous bias to chronically-implanted sites. During the coming term we hope to use this instrumentation to explore the effects of bias on tissue encapsulation of the sites. Polyimide secondary cables have also been developed for use with chronically-implanted probes in order to improve the robustness of these implants. These cables will be used in series with our normal silicon cables, which will provide greater flexibility over the final distance to the actual implant.

We are moving to demonstrate the ability to interface with these probes over a bidirectional telemetry link, eliminating all leads from the chronic assemblies. In this regard, we have completed a look at the use of subthreshold MOSFETs as shunt resistors at the amplifier inputs on the probes to prevent

DC drift in the probe input voltage (and the associated problems this drift causes in data conversion and dynamic range in completely implanted systems). Such transistor clamps appear quite suitable for this application, attenuating the input DC drift from typical sites by a factor of almost 1000 while maintaining a flat frequency response from 100Hz to over 10kHz. The attenuation and frequency passband do not appear to be significantly affected by anticipated normal process variations, and so the technique appears viable for practical use. Telemetry circuits have been designed and simulated for use with the probes, including a voltage regulator, envelope detector, power-on-reset generator, and clock generator. The system will use a forward (input) frequency of 4MHz and a reverse (output) frequency of 25MHz with a range of operation of about 1cm. It will be implemented in a 1.2µm foundry CMOS process. Simulations suggest the above circuitry will dissipate about 8.3mW at 7.5V.

The first PIA-2B probes have also been completed. The probes are fully functional and are now being readied for in-vivo testing. Operated at 5V, they offer a per-channel output resistance of less than 10K ; use of a preamplifier based on a unity-gain opamp on the next iteration of this probe should drop the output resistance to less than 1K . At 96-site active buffered probe has also been realized on the present mask set and is now ready for use.